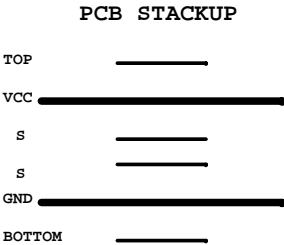
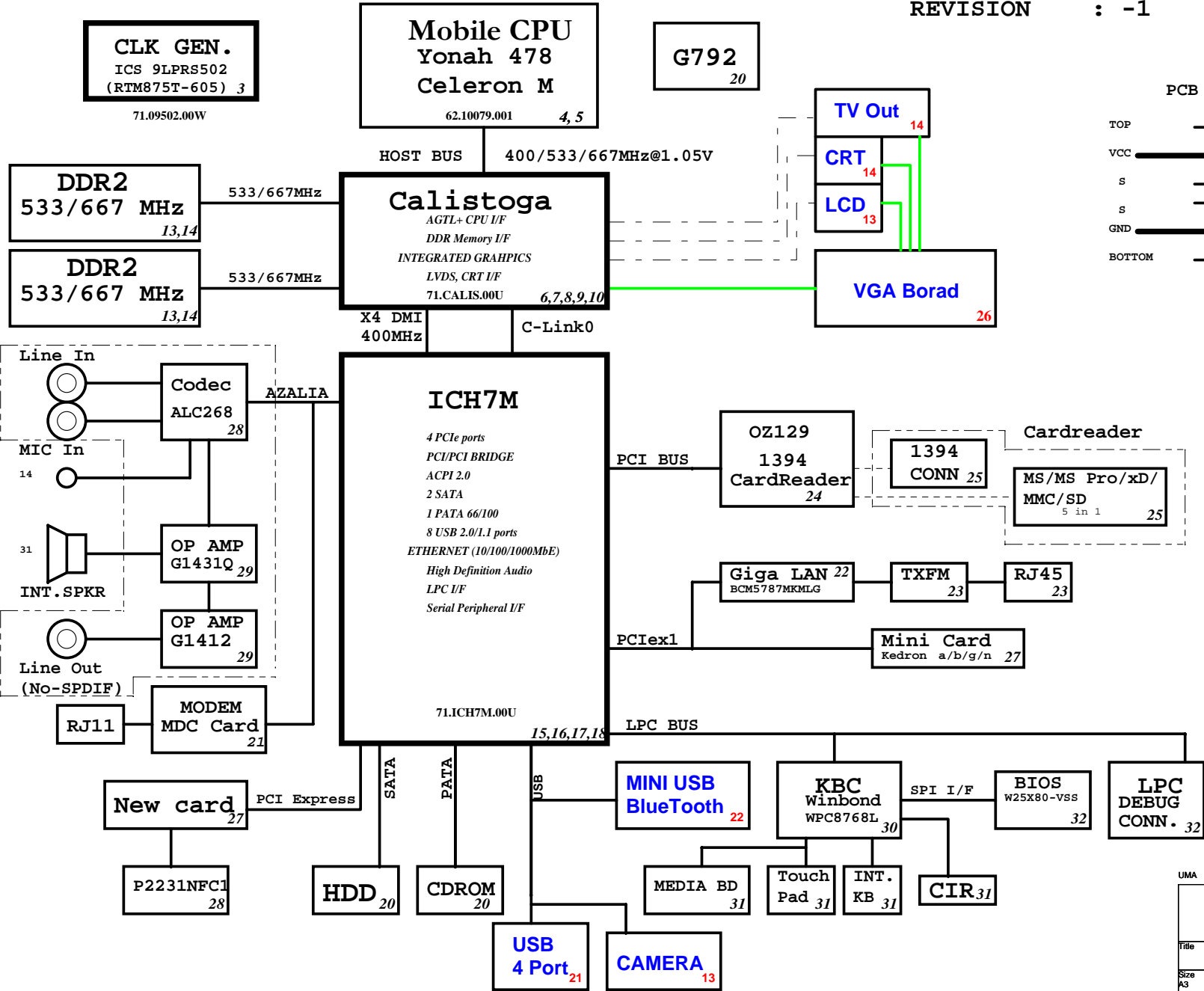


Volvi Block Diagram

Project code: 91.4U701.001
PCB P/N : 07200
REVISION : -1



SYSTEM DC/DC MAX8744 36	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3V_S5
SYSTEM DC/DC MAX8717 37	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D05V_S0
TPS51100 39	
1D8V_S3	DDR_VREF
APL5312 39	
3D3V_S0	2D5V_S0
APL5912 38	
1D8V_S3	1D5V_S0

Intersil CHARGER MAX8731 40	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 4.0A UP+5V 5V 100mA

CPU DC/DC MAX8770 35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0-1.3V 48A

ICH7M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting PWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH7M IDE Integrated Series
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

PCIE Routing

LANE1	LAN BCM5787M
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

USB Table

USB ports definition	
Pair	Device
0	USB1
1	USB3
2	USB2
3	USB4
4	MINICARD
5	BlueTooth
6	CCD
7	NewCard

PCI Routing

	IDSEL	INT	REQ	GNT
OZ129	AD22	INT_PIRQ#	PCI_REQ#0	PCI_GNT#0

ICH7M Integrated Pull-up
and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

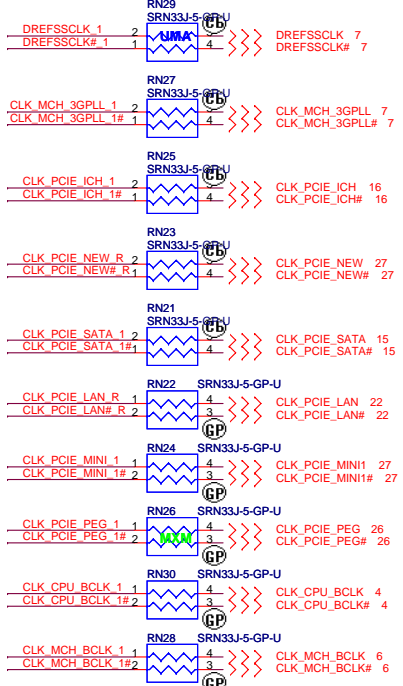
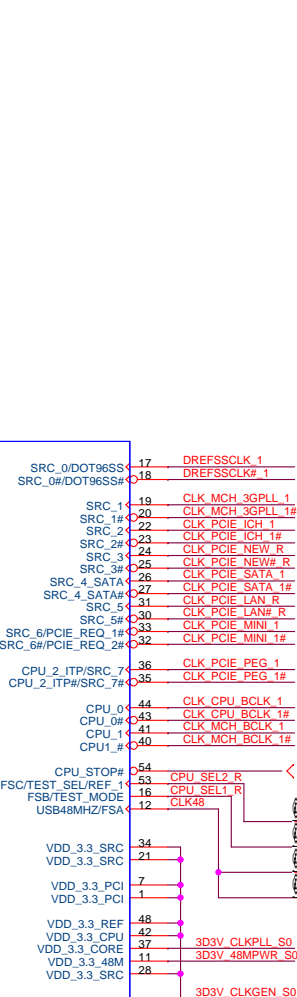
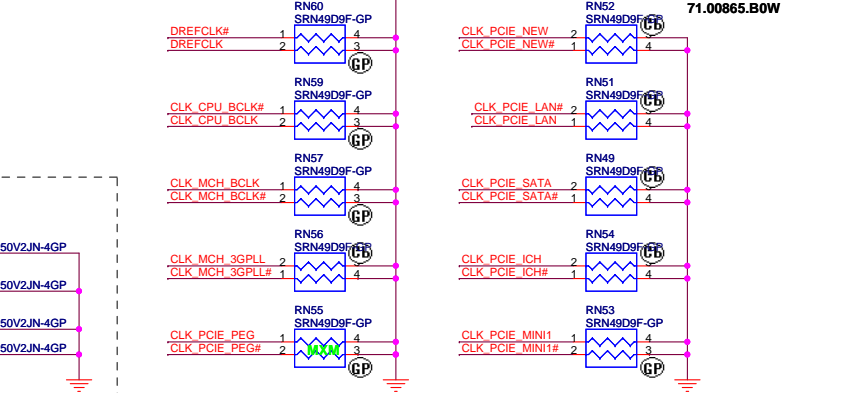
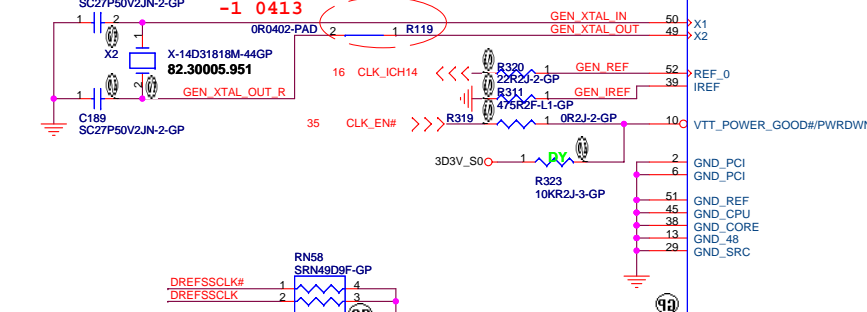
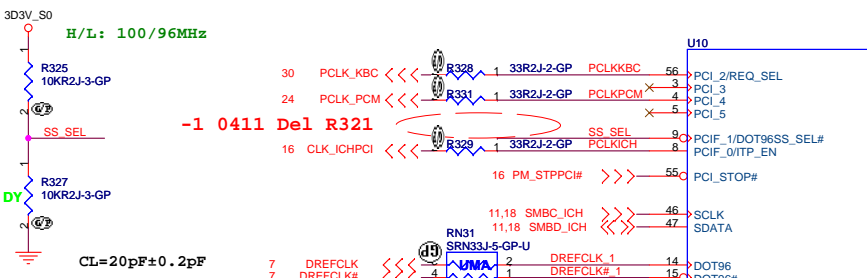
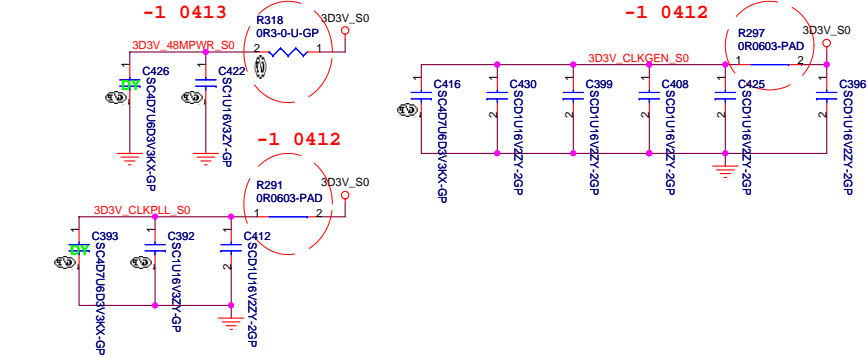
Crestline Strapping Signals and
Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

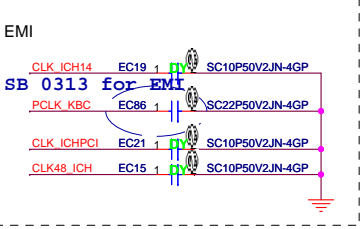
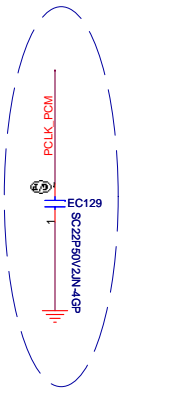
NOTE: All strap signals are sampled with respect to the leading
edge of the Crestline GMCH PWORK in signal.

UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reference			
Size A3	Document Number	Volvi	Rev -1
Date: Wednesday, April 18, 2007	Sheet	2	of 42



SB 0313 for EMI



FSC	FSB	FSA	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

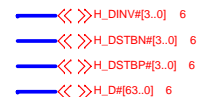
UMA

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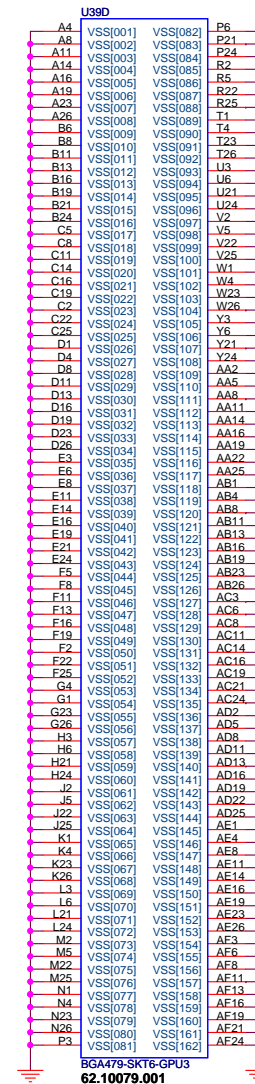
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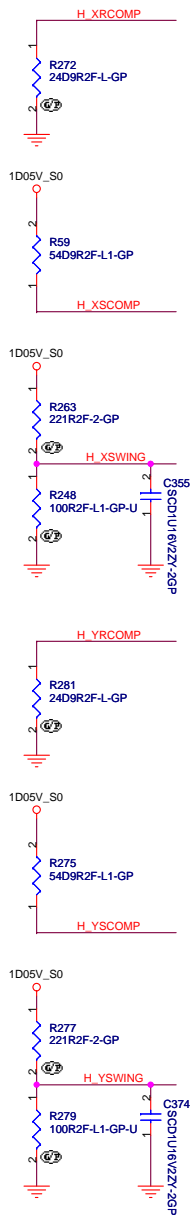
Size: Document Number: **Volvi** Rev: -1

Date: Wednesday, April 18, 2007 Sheet 3 of 42

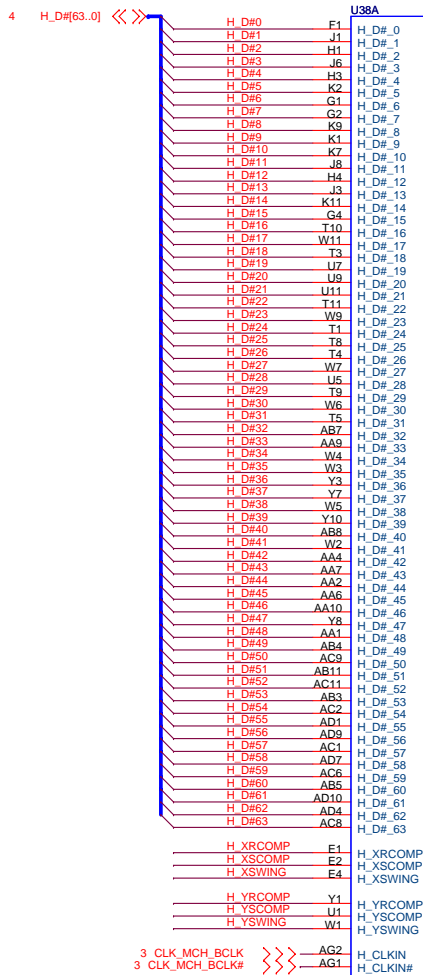


UMA			
緯創資通		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
		CPU (1 of 2)	
Size	Document Number	Volvi	Rev -1
Date:	Wednesday, April 18, 2007	Sheet 4	of 42

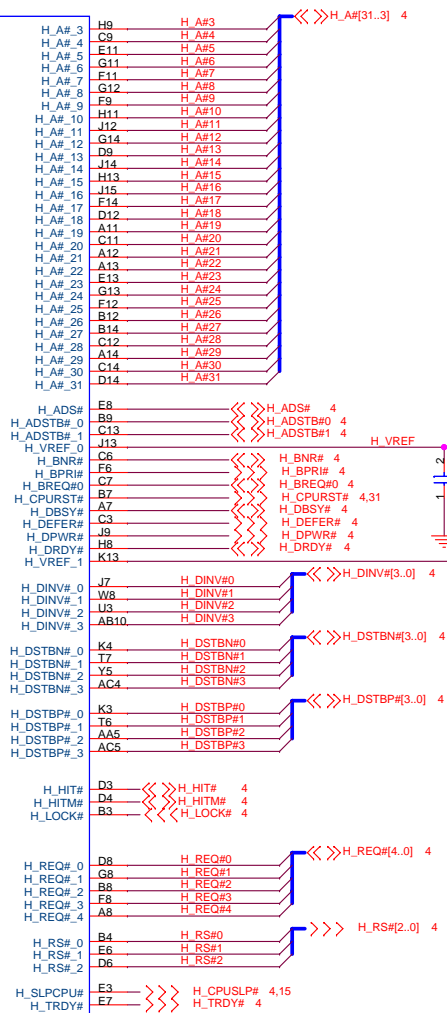




Place them near to the chip (< 0.5")



HSO7

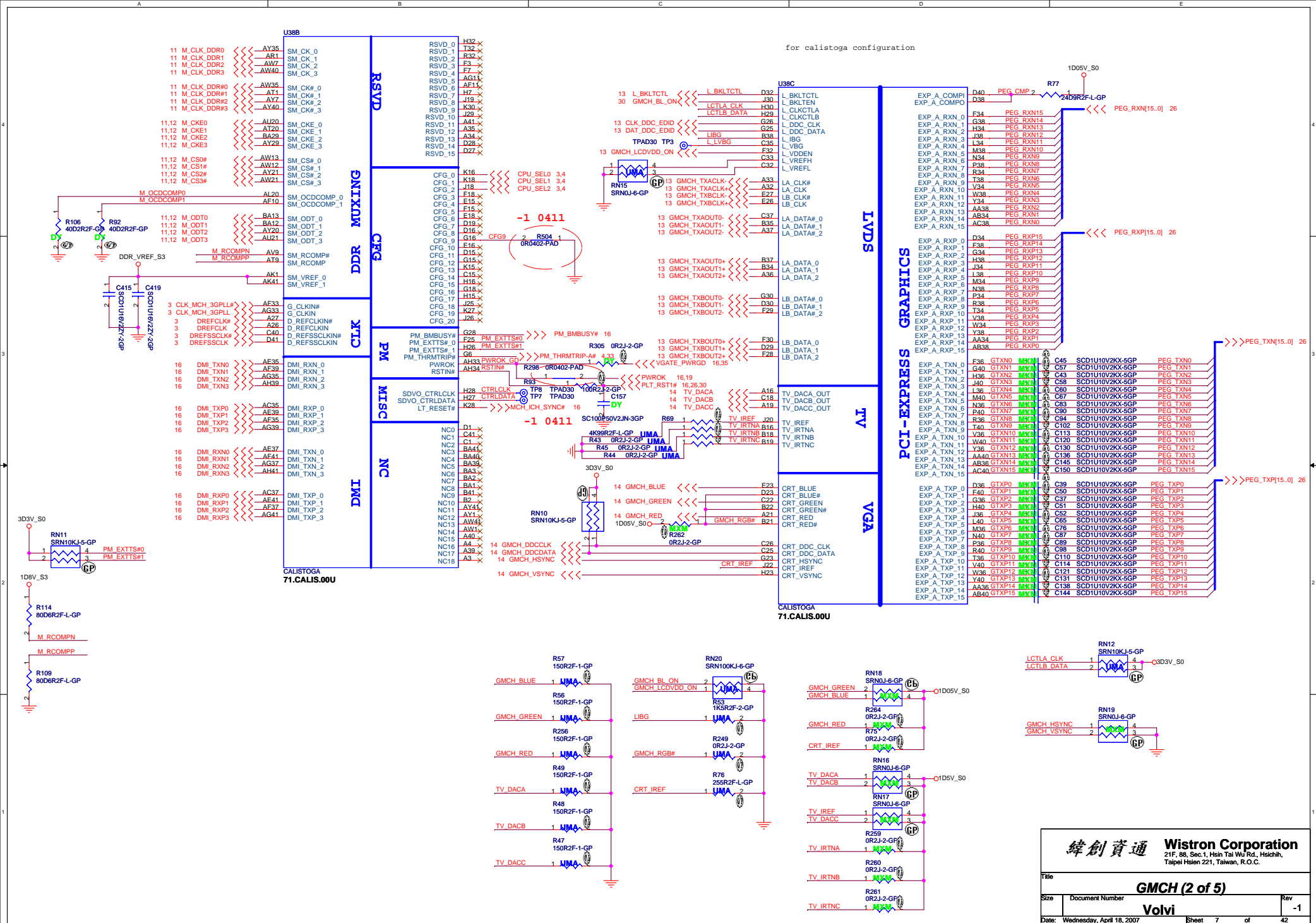


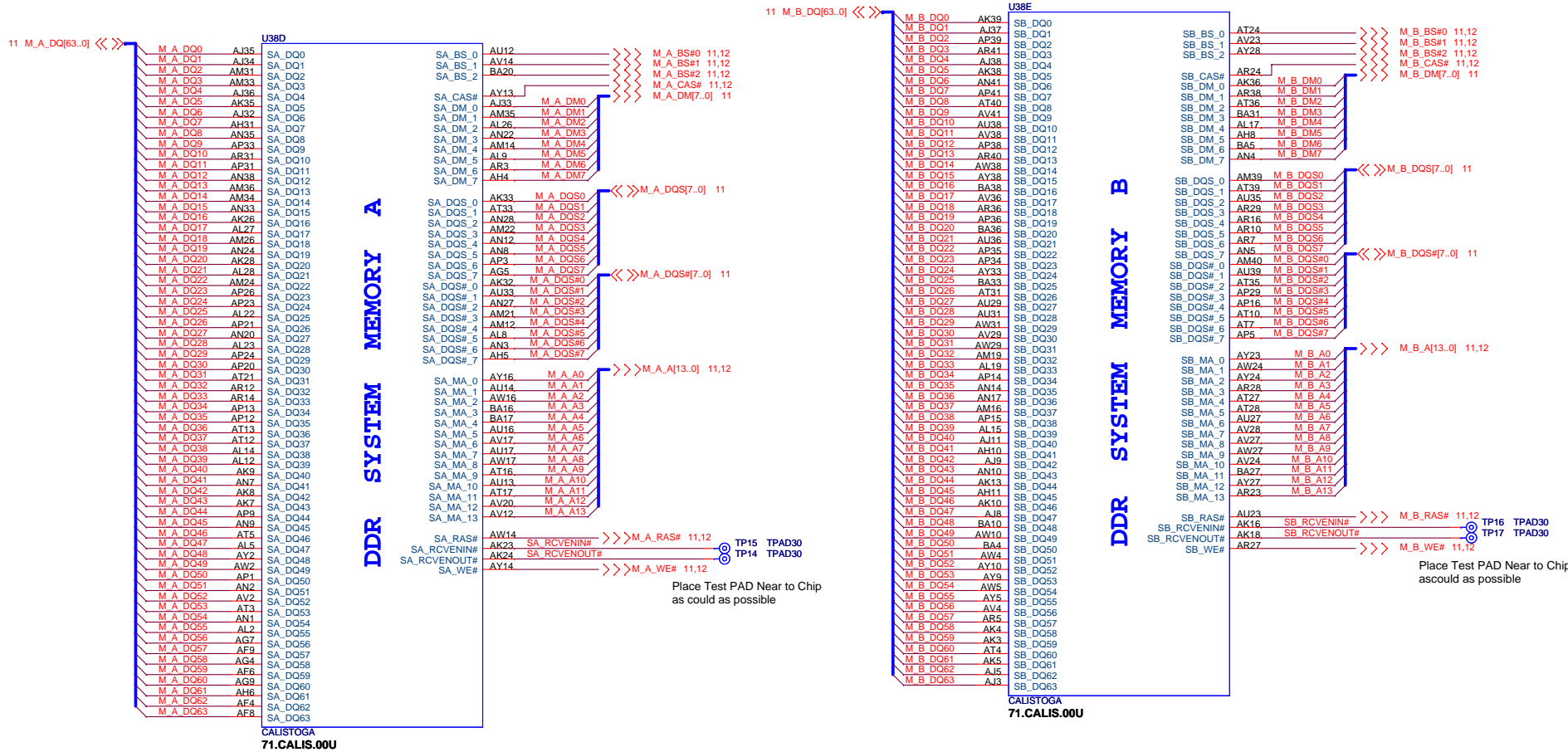
CALISTO
71.CALIS.00U

DIS :PM945 KI.94501.006
UMA :GM945 KI.94501.005

UMA

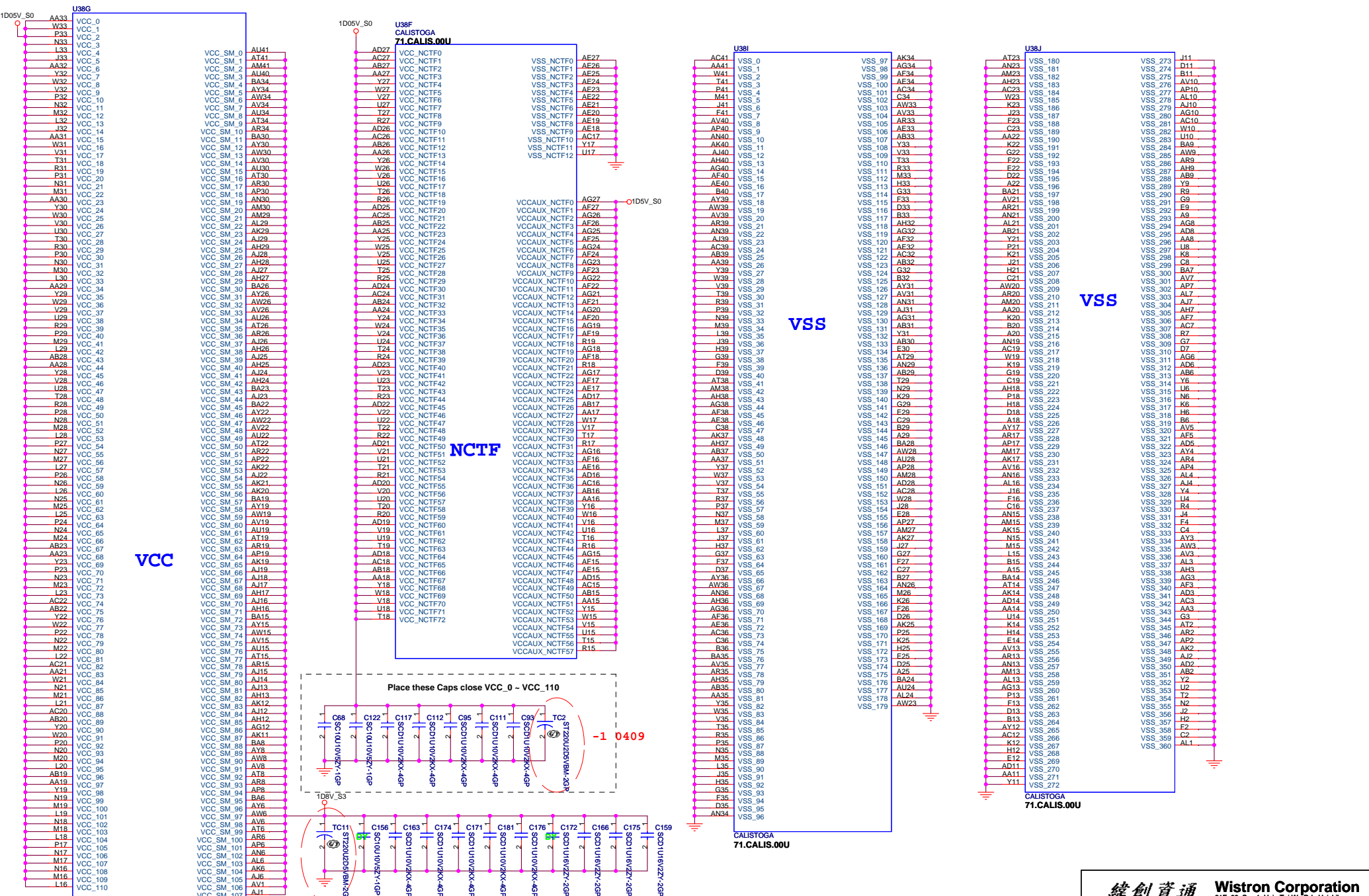
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
GMCH (1 of 5)		
Size	Document Number	Rev
		-1
Date: Wednesday, April 18, 2007		Sheet 6 of 42

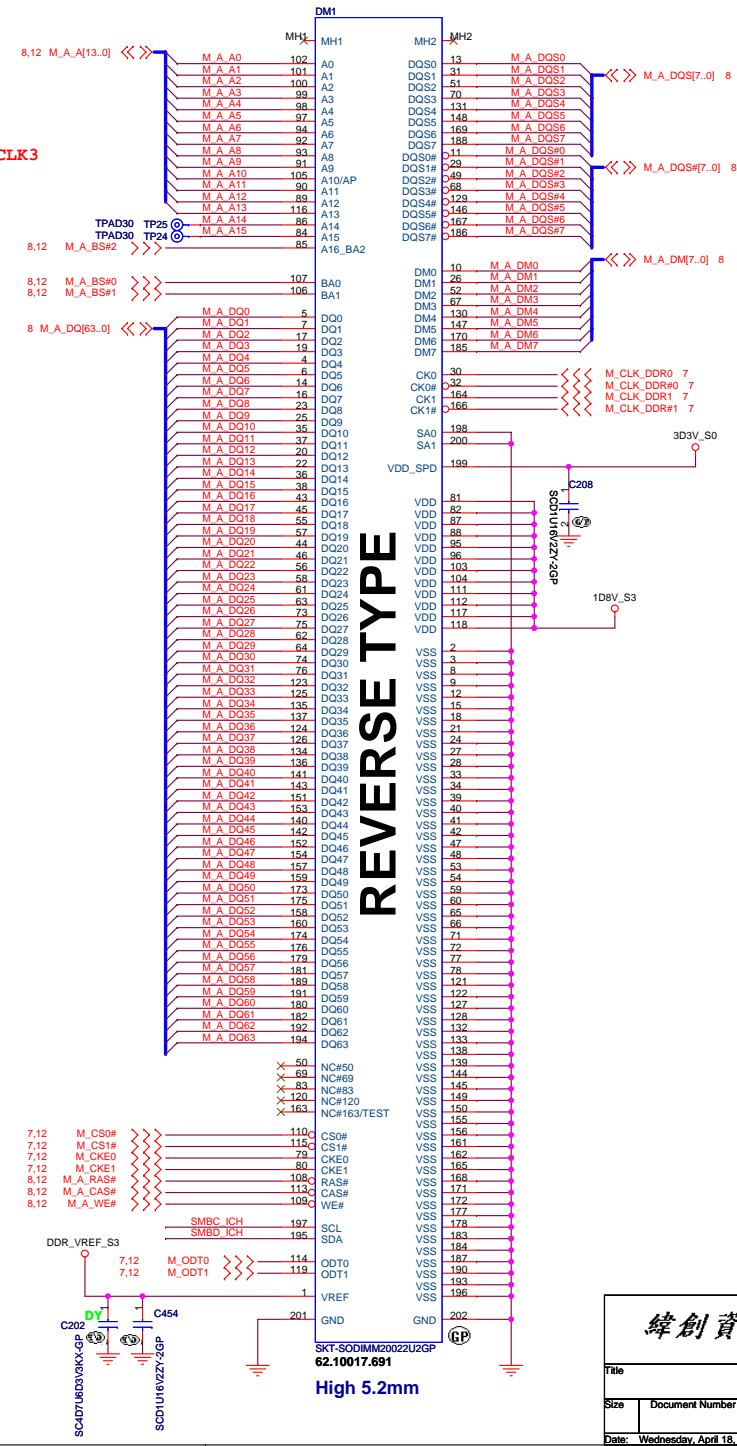
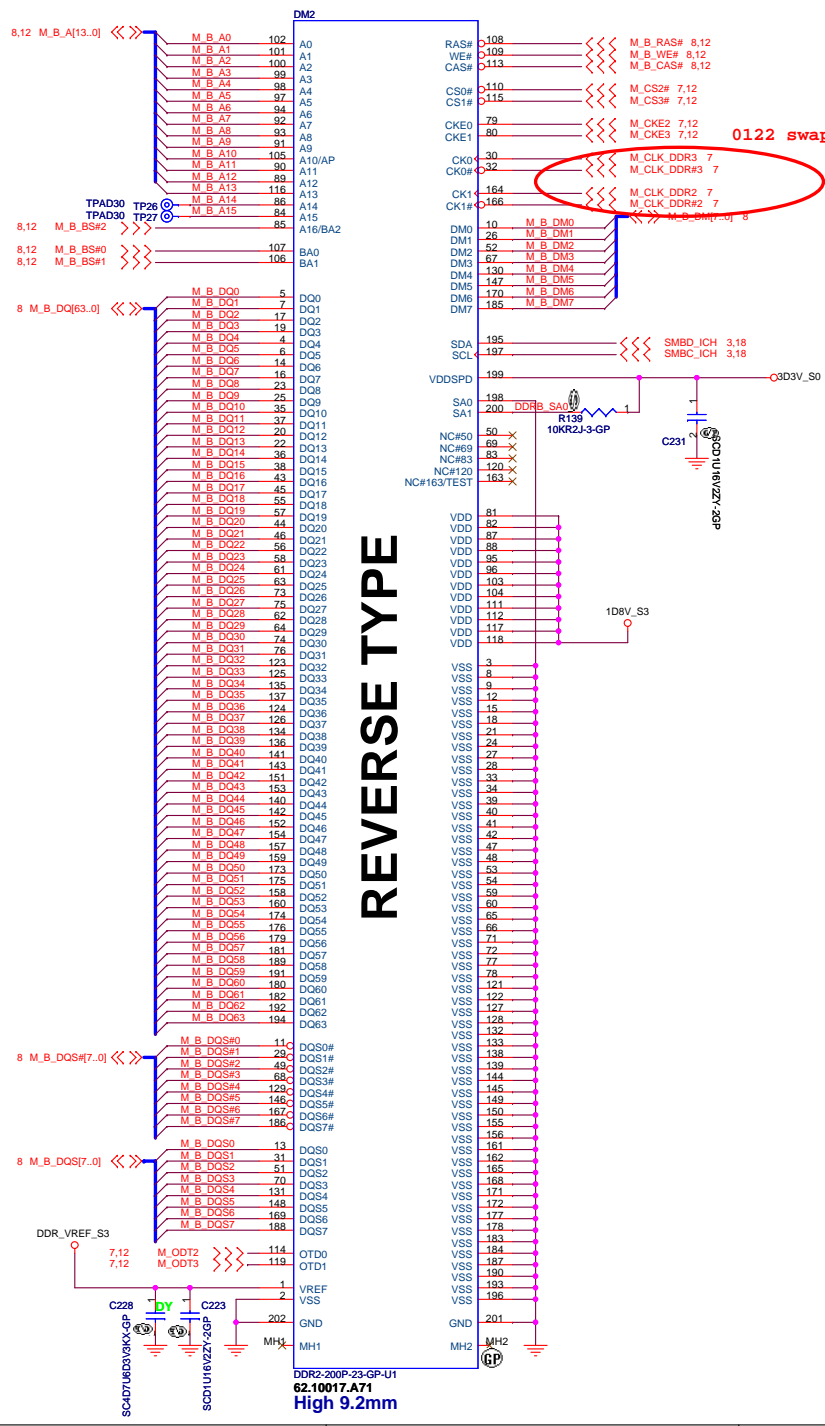




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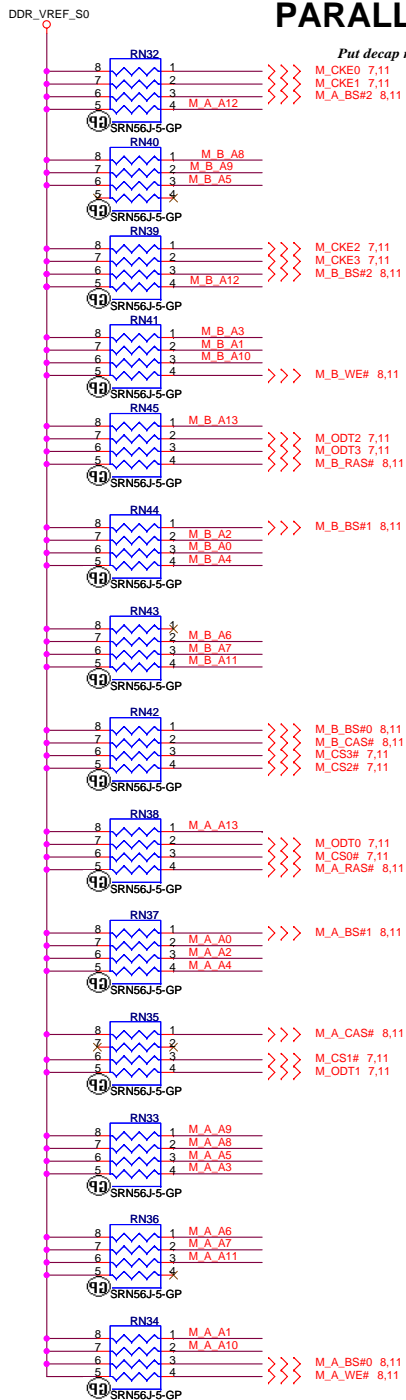
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GMCH (3 of 5)		
Size	Document Number	Rev
		-1
Date: Wednesday, April 18, 2007		
Sheet 8 of 42		



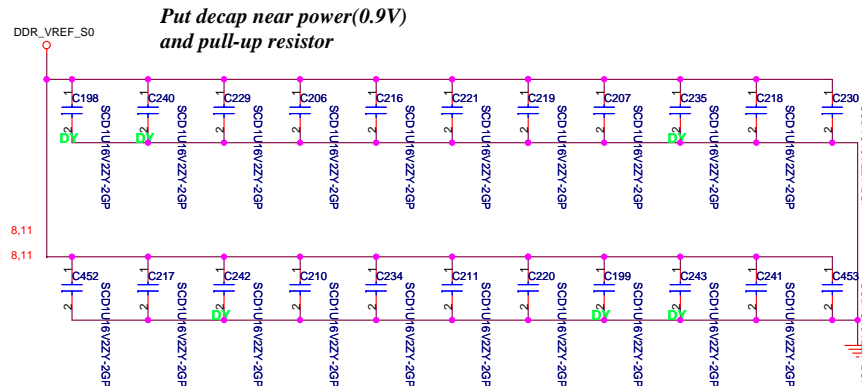


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Title	
DDR2 Socket	
Size	Document Number
Volvi	
Date: Wednesday, April 16, 2007	Rev -1
Sheet 11	of 42

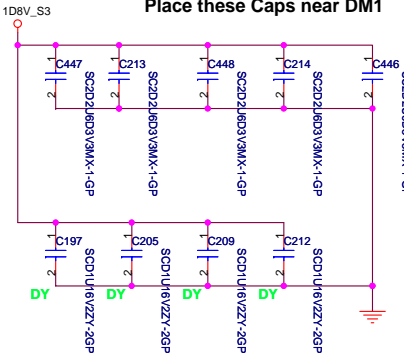
PARALLEL TERMINATION



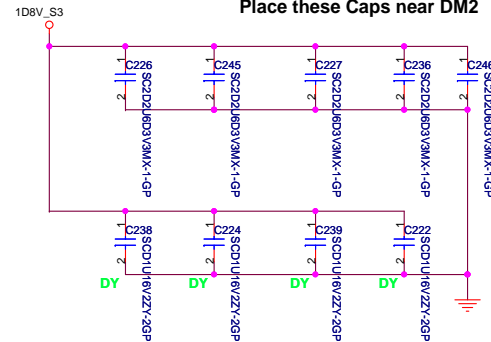
Decoupling Capacitor



Place these Caps near DM1

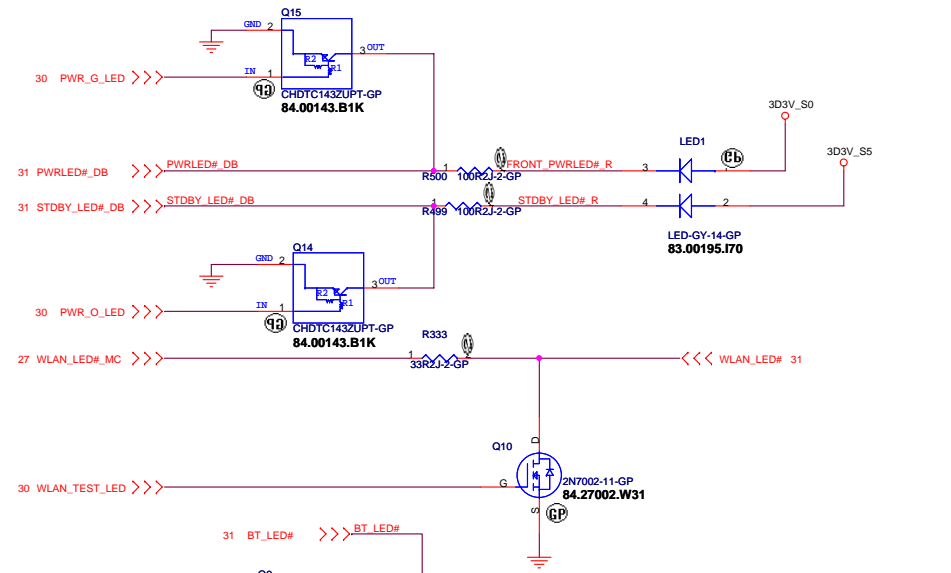
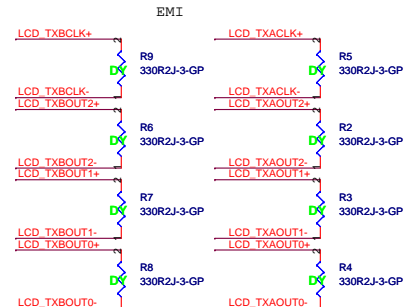


Place these Caps near DM2



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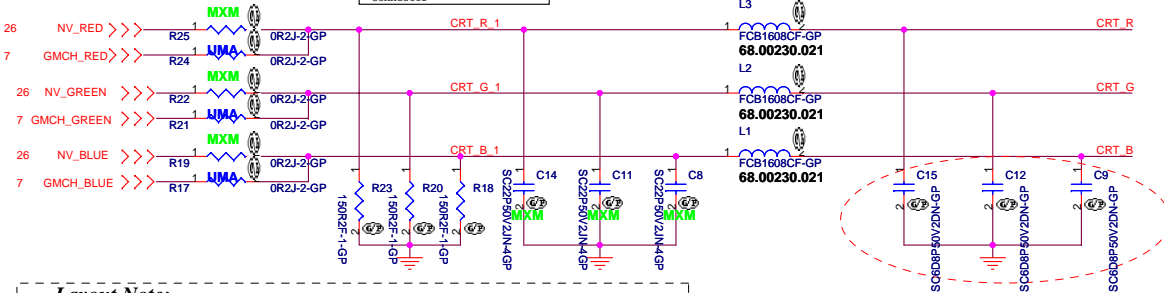
Title			
DDR2 Termination Resistor			
Size	Document Number		Rev
	Volvi		-1
Date: Wednesday, April 18, 2007		Sheet 12 of 42	

[illegible]

CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

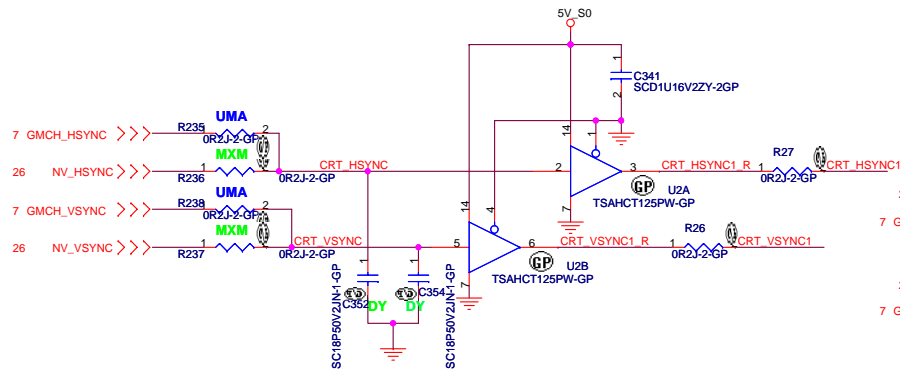
Ferrite bead impedance: 10 ohm@100MHz



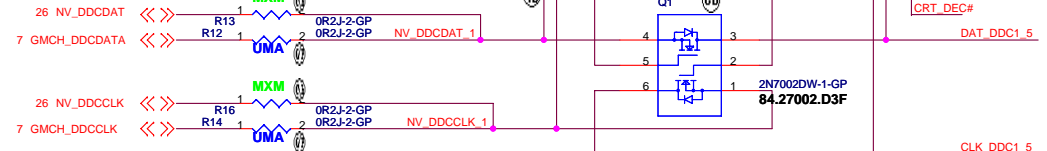
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

C15 to 18P
C12 to 27P
C9 to 27P
For ATI MXM M66M R,G,B

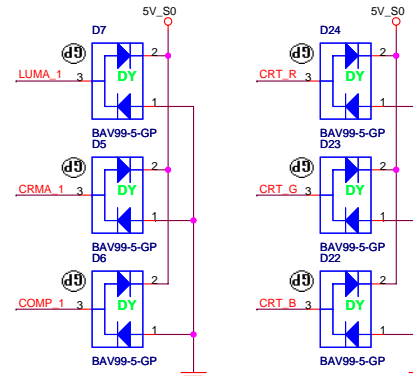
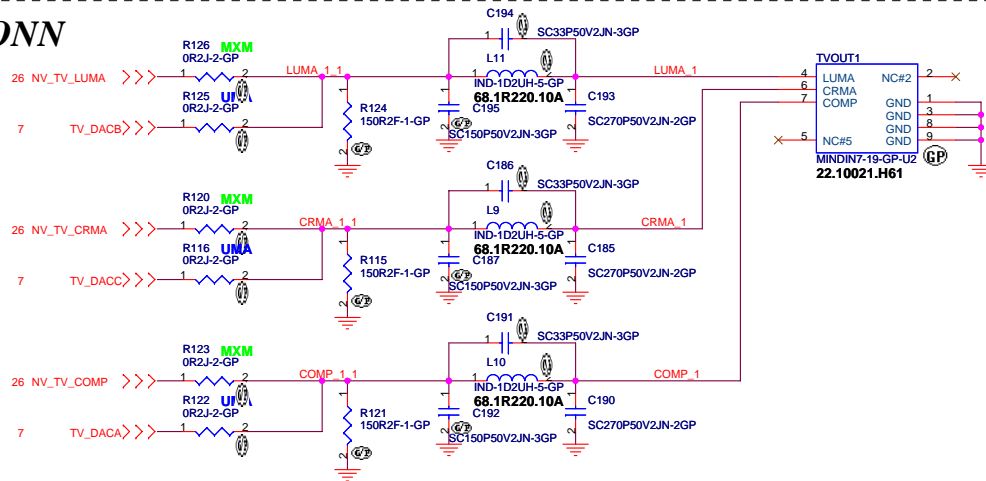
Hsync & Vsync level shift



DDC_CLK & DATA level shift



TV CONN

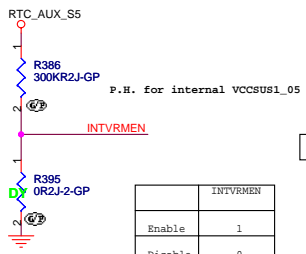
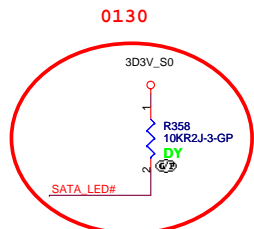
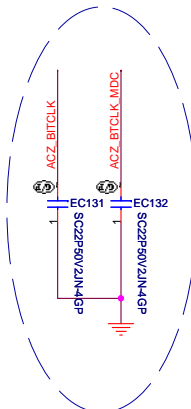


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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CRT/TV Connector	
Size	Document Number
Volvi	
Date: Wednesday, April 18, 2007	Sheet 14 of 42

SB 0305

RTC circuitry

SB 0313 for EMI

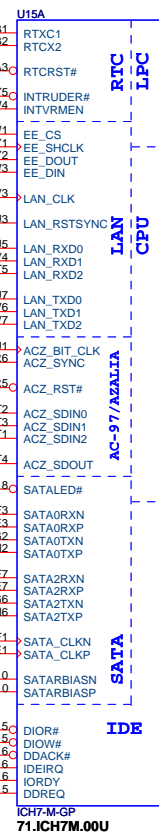
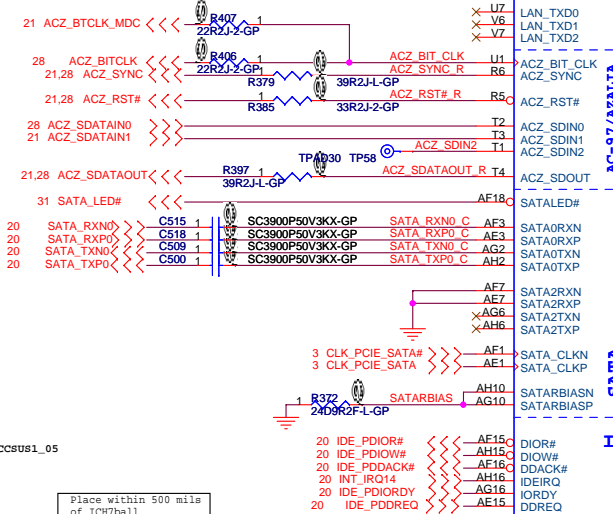
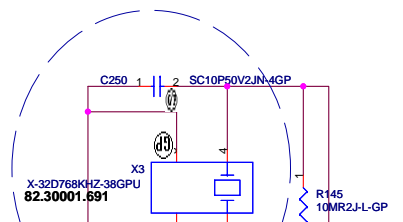


Placement Note:
Distance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.

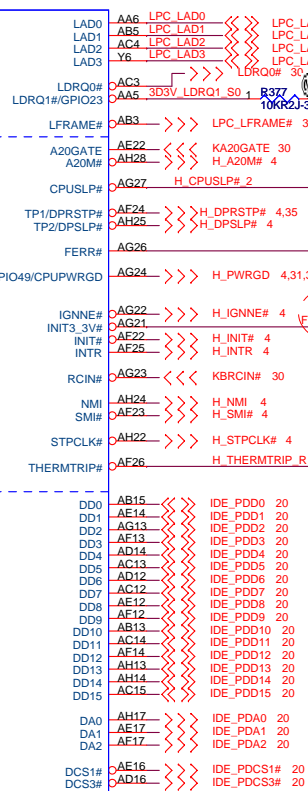
	INTVRMEN
Enable	1
Disable	0

Place within 500 mils of ICH7ball

SB 0305



Change to KI.80101.017



Open R for Dothan A step
Shunt for Dothan B step
& all Yonah

Layout Note: R568 needs to be placed
within 2" of ICH7, R568 must be placed
within 2" of R169 w/o stub.

UMA

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Title

ICH7-M (1 of 4)

Size

Document Number

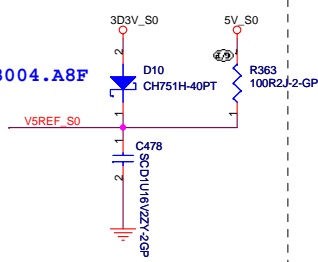
Rev

-1

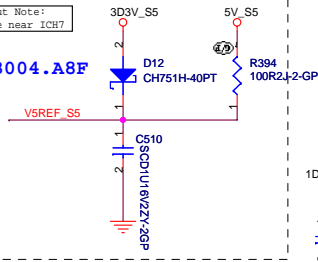
Date: Wednesday, April 18, 2007

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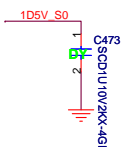
2nd 83.R3004.A8F



2nd 83.R3004.A8F



*Within a given well, V5REF needs to be up before the corresponding 3.3V rail



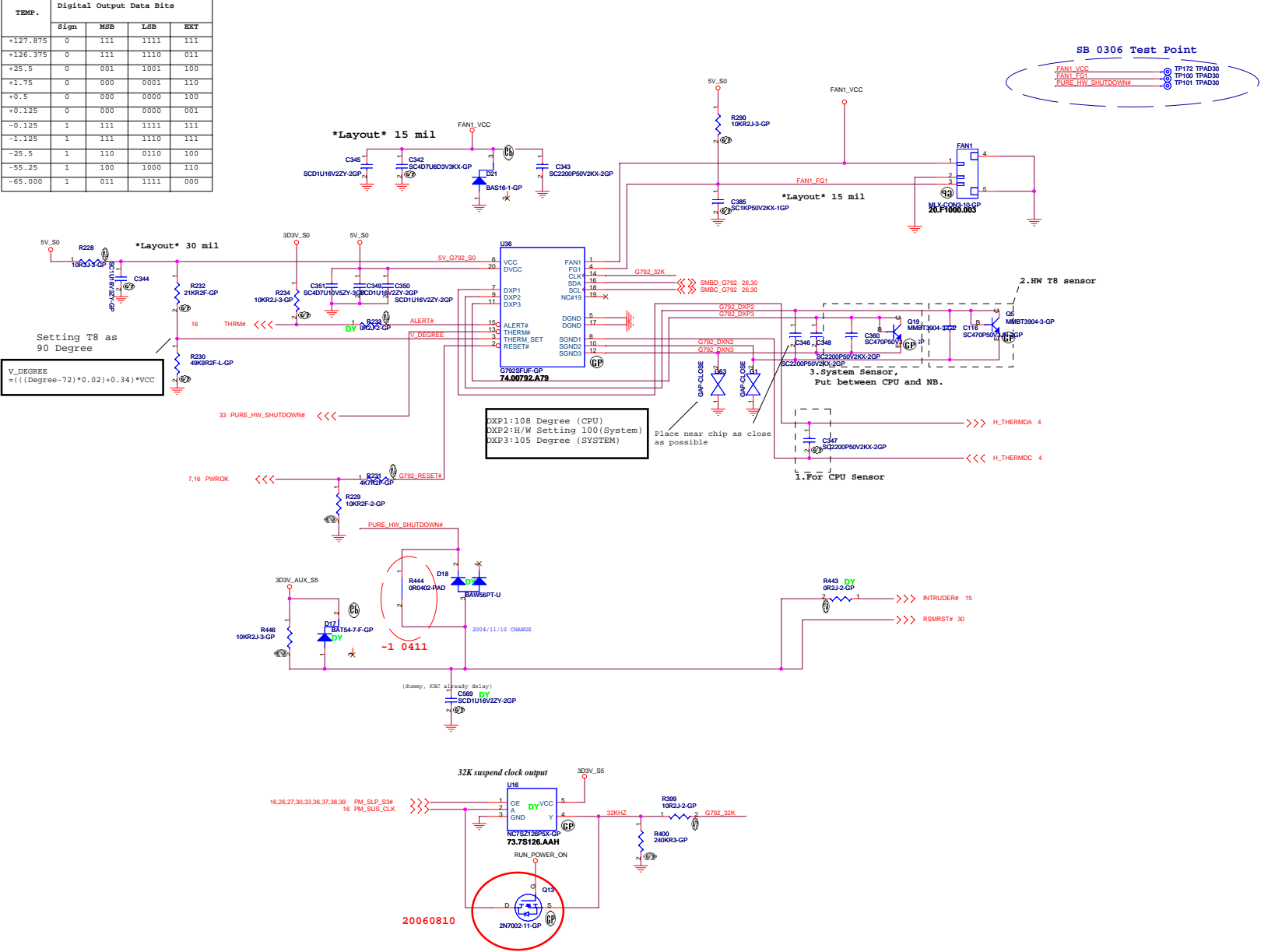
ICH7-M-GP
71.ICH7M.00U

Layout Note:
Place near pin AA19

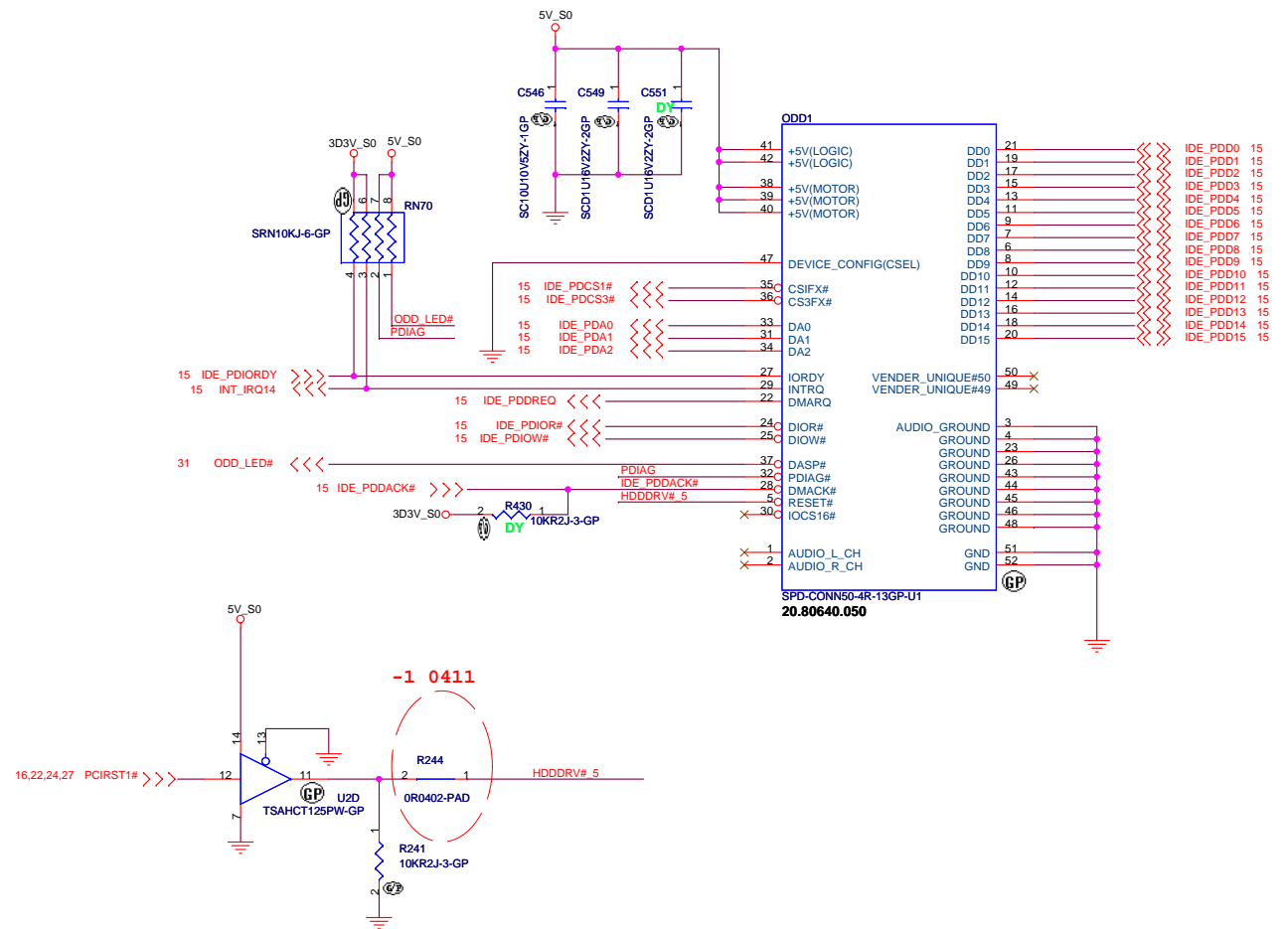
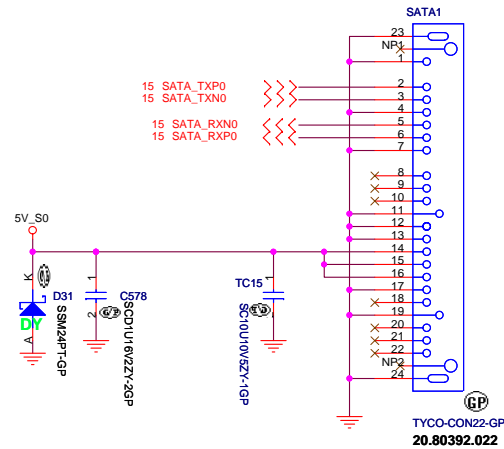
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Title			ICH7-M (3 of 4)
Size	Document Number	Rev	-1
Date: Wednesday, April 18, 2007			Sheet 17 of 42

TEMP.	Digital Output Data Bits				
	Sign	MSB	LSB	EXT	
+127.875	0	111	1111	111	
+126.375	0	111	1110	011	
+25.5	0	001	1001	100	
+1.75	0	000	0001	110	
+0.5	0	000	0000	100	
+0.125	0	000	0000	001	
-0.125	1	111	1111	111	
-1.125	1	111	1110	111	
-25.5	1	110	0110	100	
-55.25	1	100	1000	110	
-65.000	1	011	1111	000	



ODD Connector



UMA

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Title

HDD and CDROM

Size

Document Number

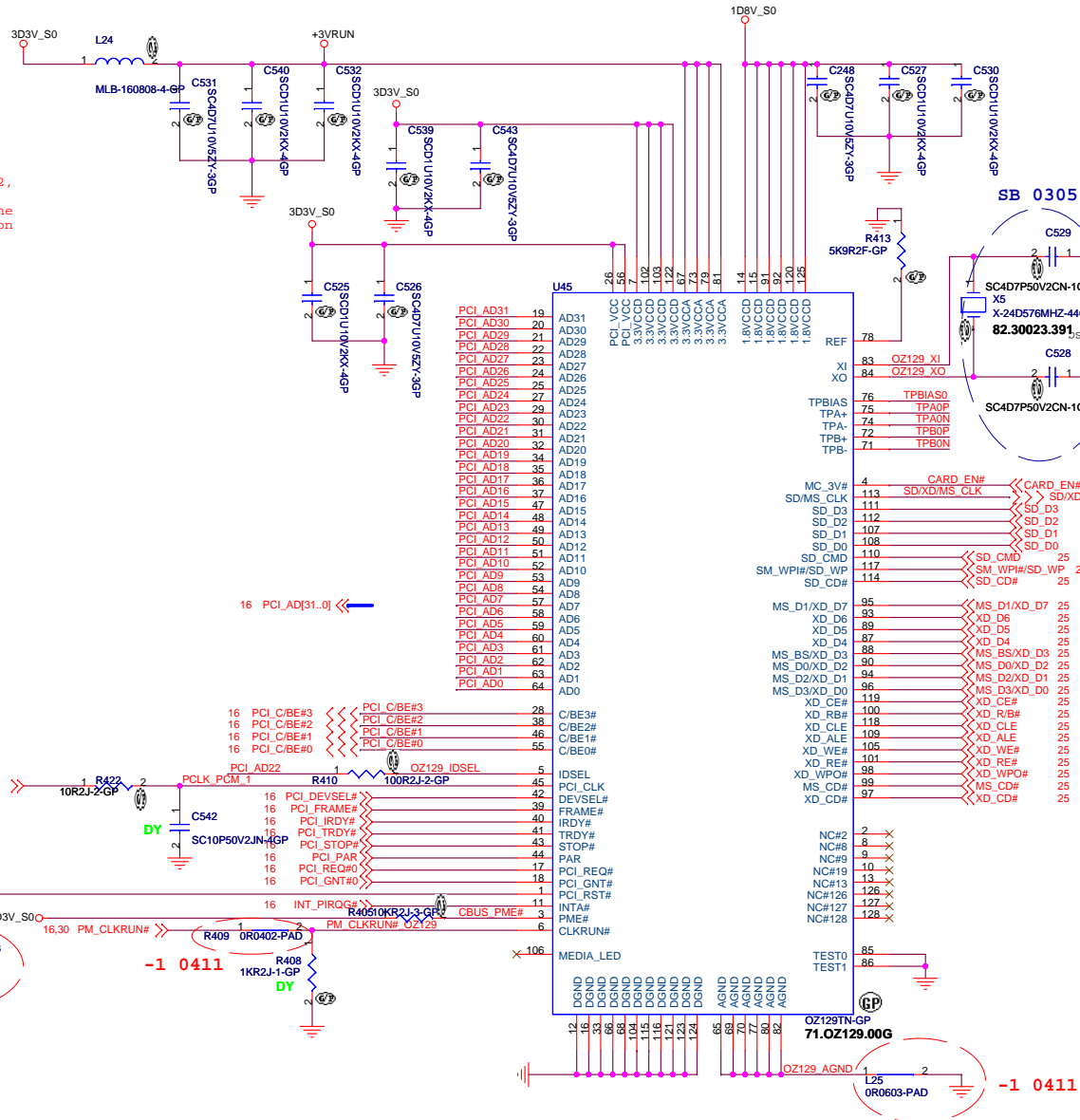
Volvi

-1

Date: Wednesday, April 18, 2007

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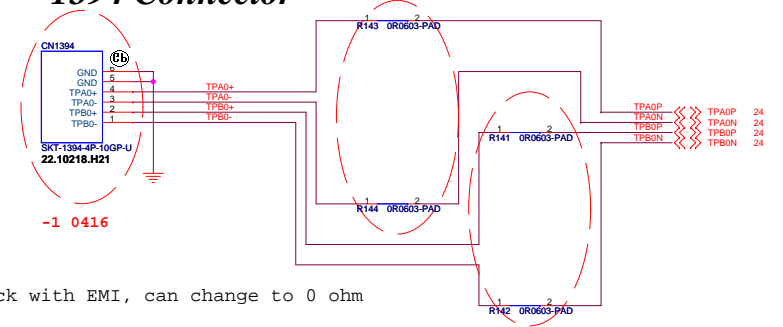
TPBIAS0			
TPA0P	⌵	⌶	TPA0P 25
TPA0N	⌵	⌶	TPA0N 25
TPB0P	⌵	⌶	TPB0P 25
TPB0N	⌵	⌶	TPB0N 25

UMA

Title			
OZ129T			
Size	Document Number		Rev
	Volvi		-1
Date:	Wednesday, April 18, 2007	Sheet 24 of	42

1394 Connector

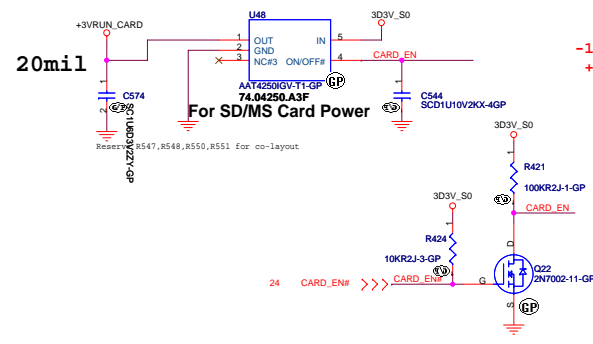
-1 0411 del L22 and L23



-1 0416

check with EMI, can change to 0 ohm

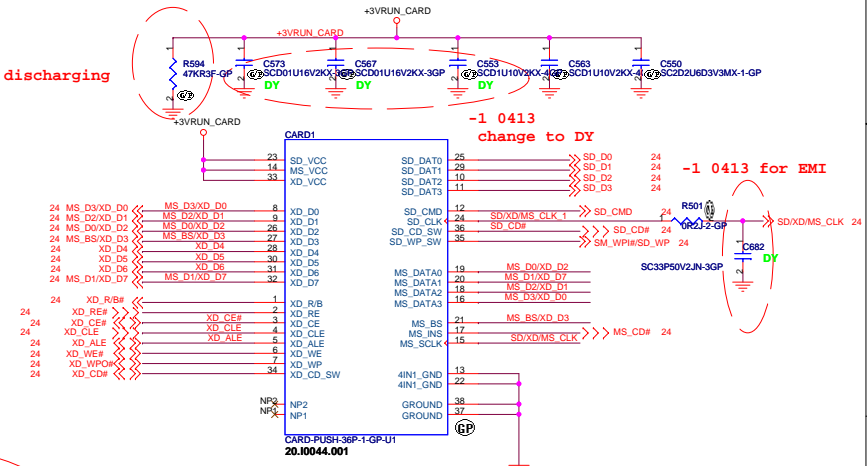
20mil



For SD/MS Card Power

-1 0413

+3VRUN_CARD discharging

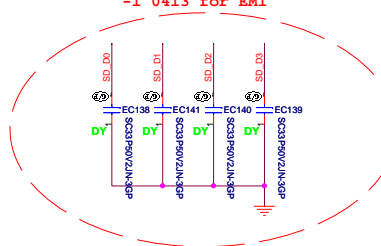


-1 0413

change to DY

-1 0413 for EMI

-1 0413 for EMI



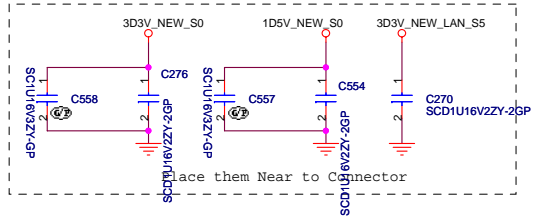
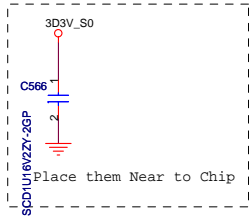
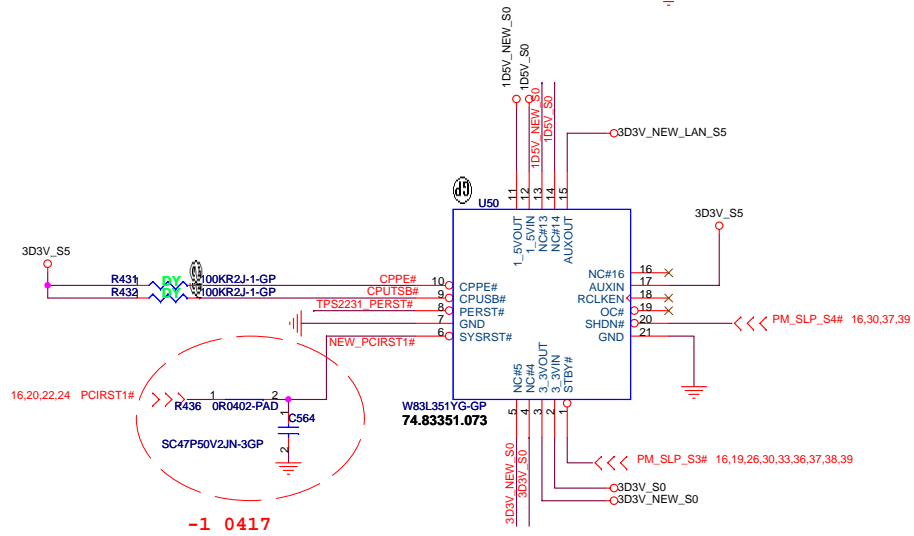
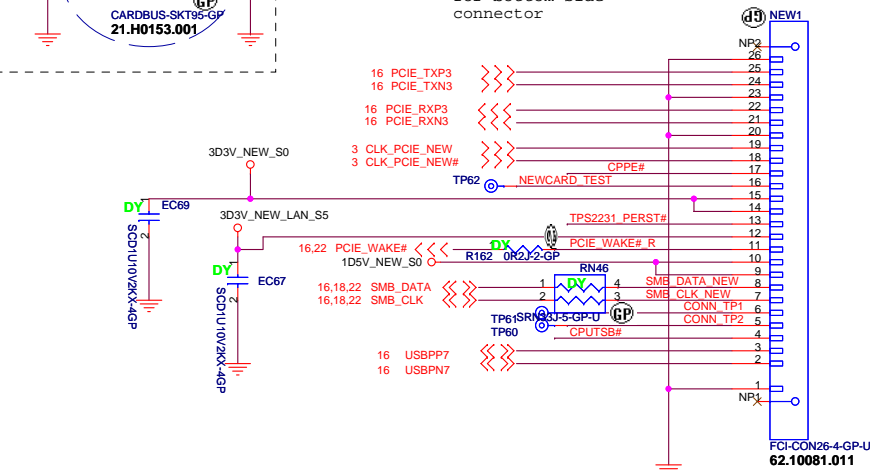
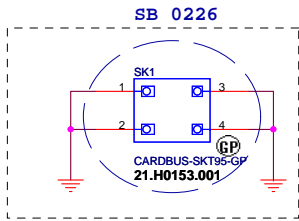
UMA

緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
Title 1394 / CARD READER	
Size Document Number	Rev -1
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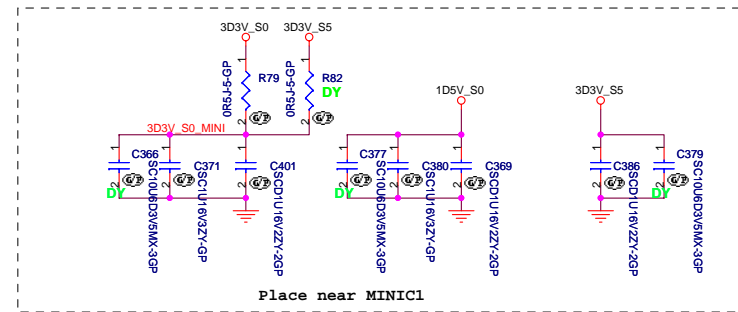
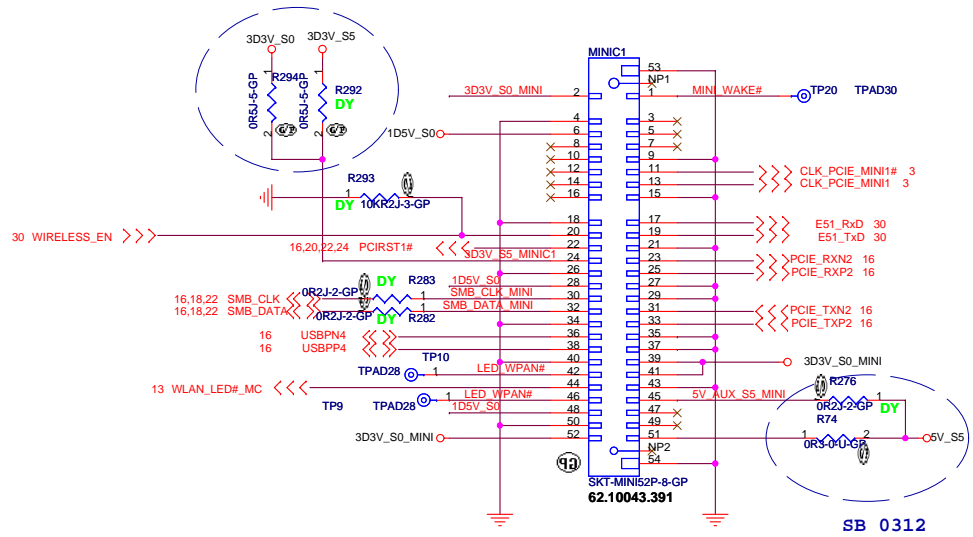
Mini Card Connector

NEWCARD Connector

Reserve the symbol
for bottom side
connector



SB 0312



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Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

MINI CARD / NEW CARD

Size

	Document Number
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Volvi

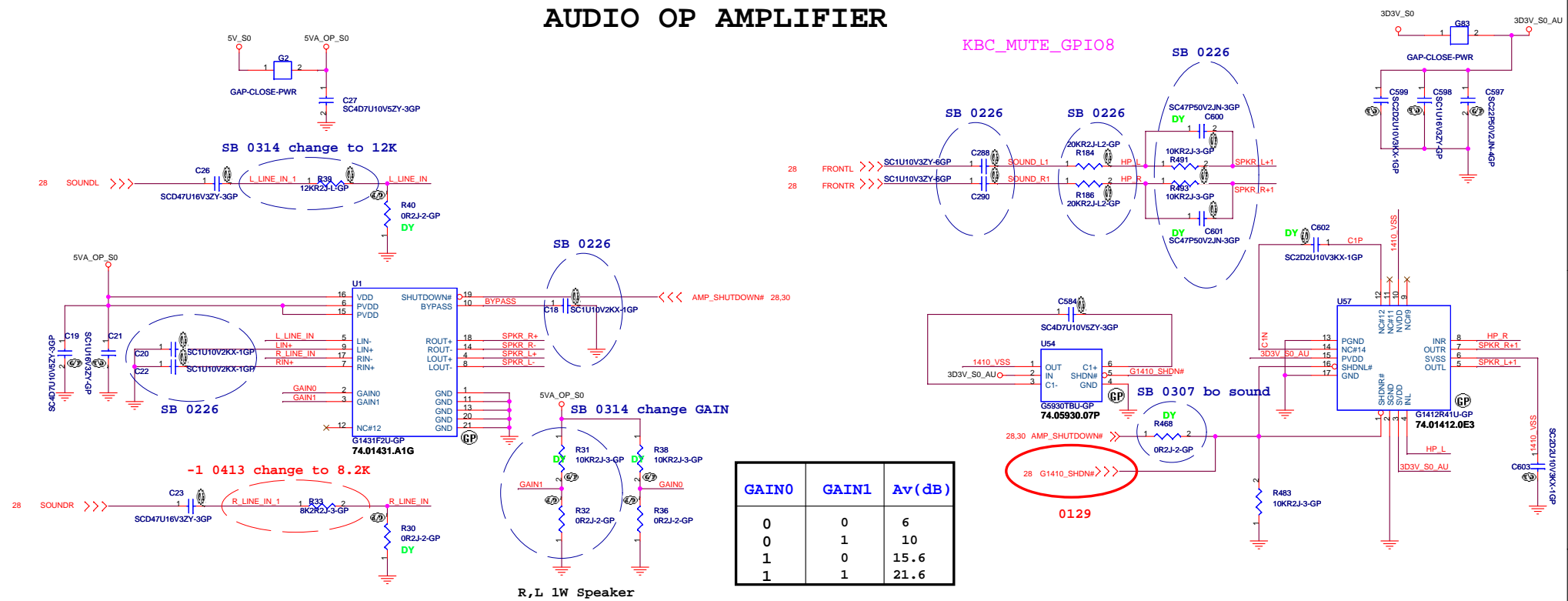
Rev

Date: Wednesday, April 18, 2007

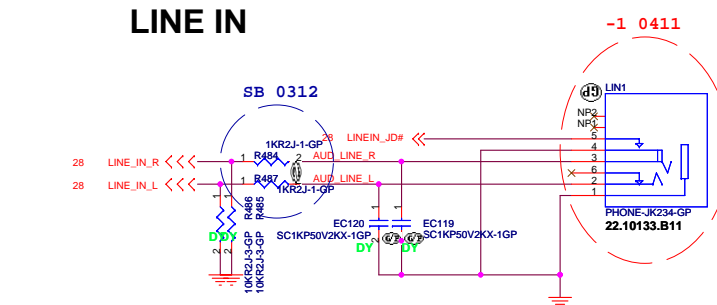
Sheet 27

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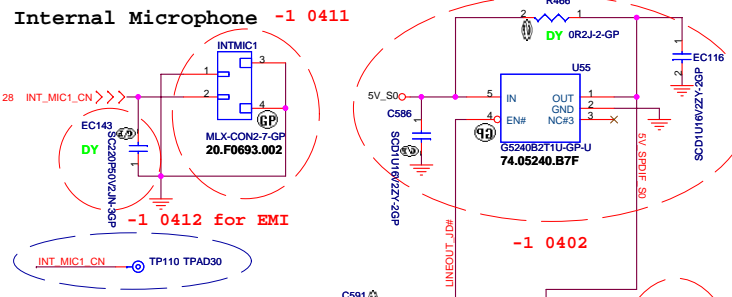
AUDIO OP AMPLIFIER



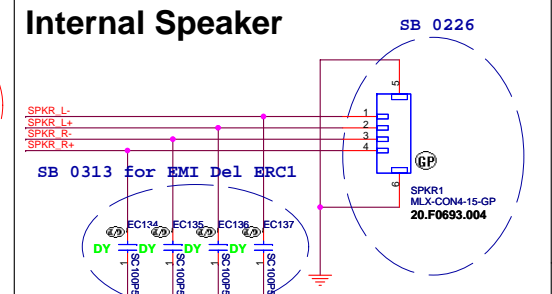
LINE IN



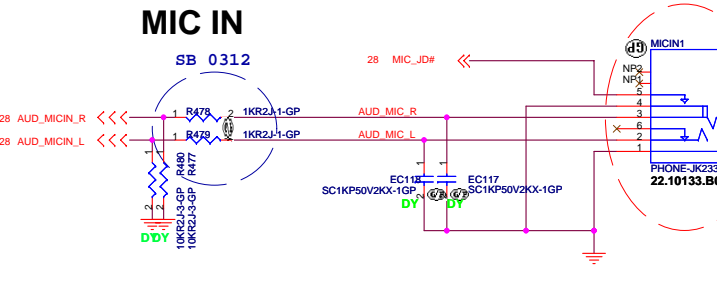
Internal Microphone -1 0411



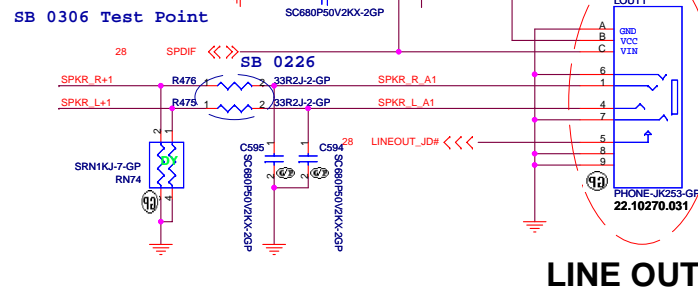
Internal Speaker



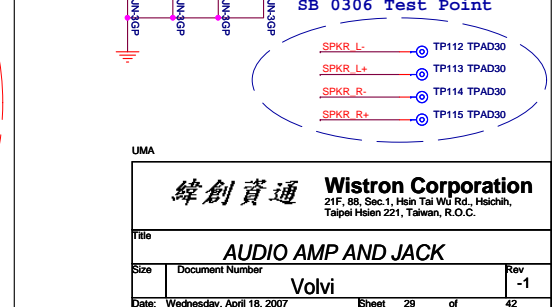
MIC IN



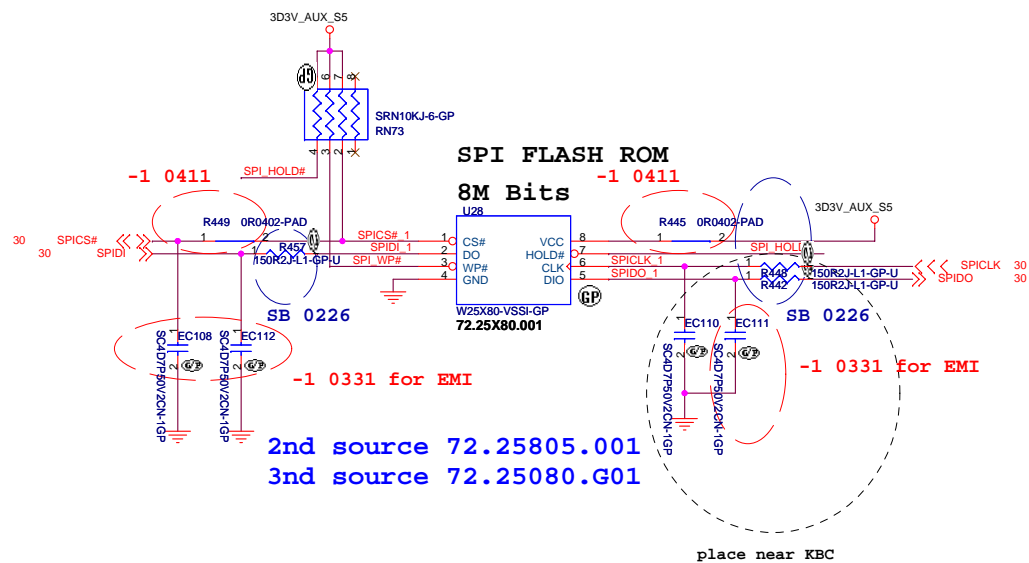
SB 0306 Test Point



LINE OUT



UMA			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BUTTONs / KB / TOUCHPAD			
Size	Document Number	Volvi	Rev -1
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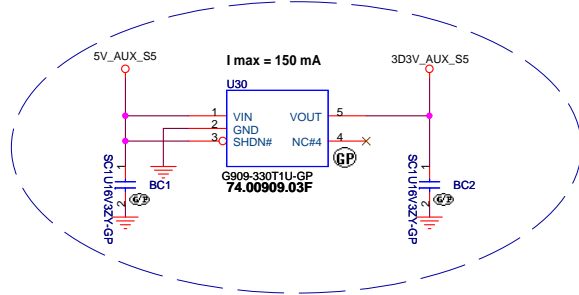


UMA

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BIOS			
Size A3	Document Number Volvi		Rev -1
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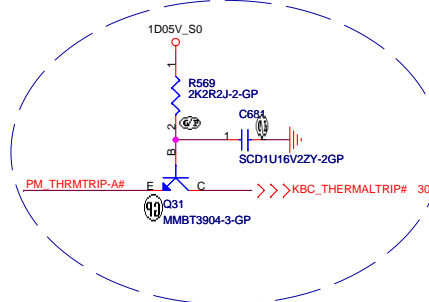
Aux Power

3D3V_AUX_S5

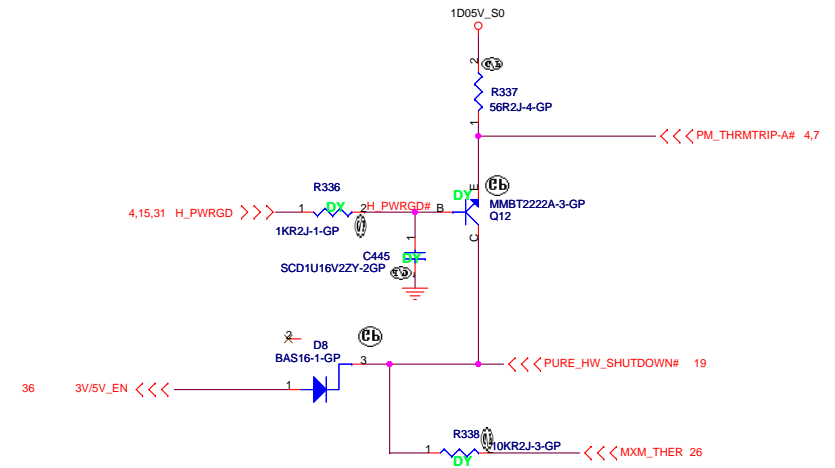
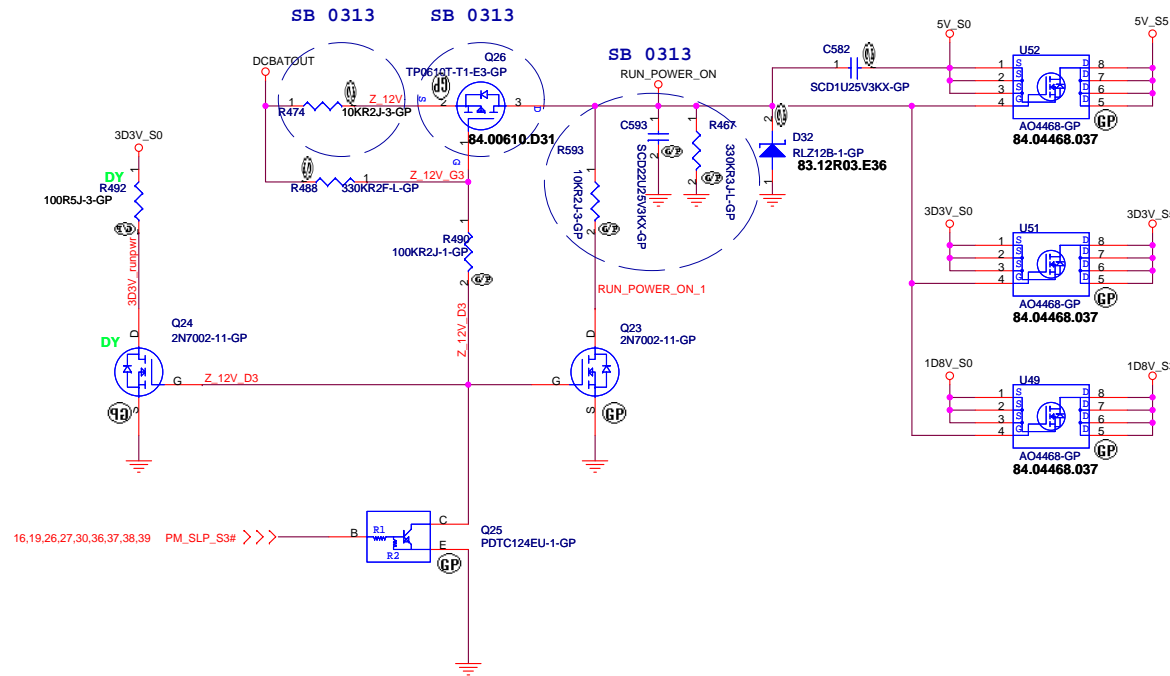


SB 0226 Del R458,R460,BC3 (SA)

SB 0216



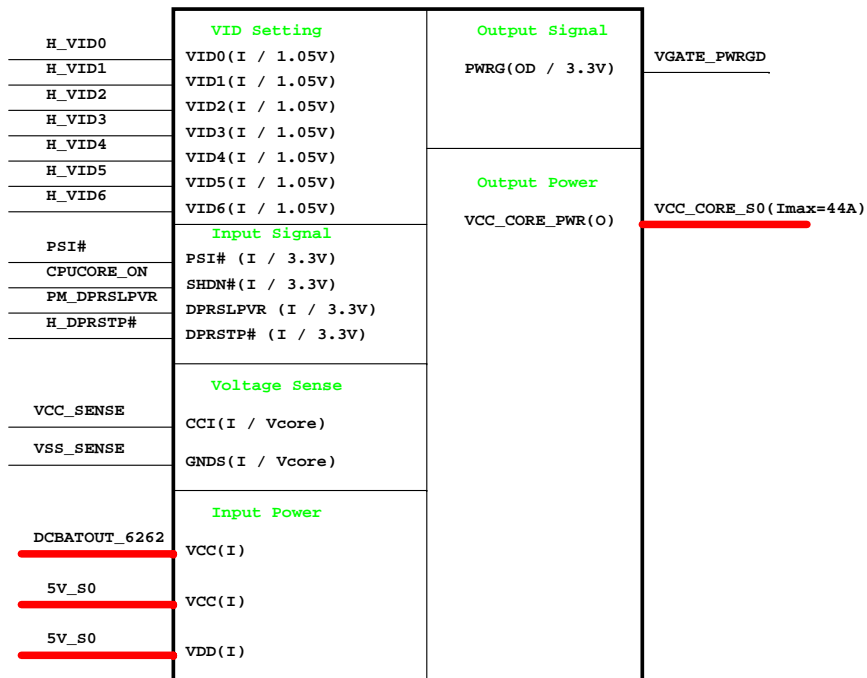
Run Power



UMA

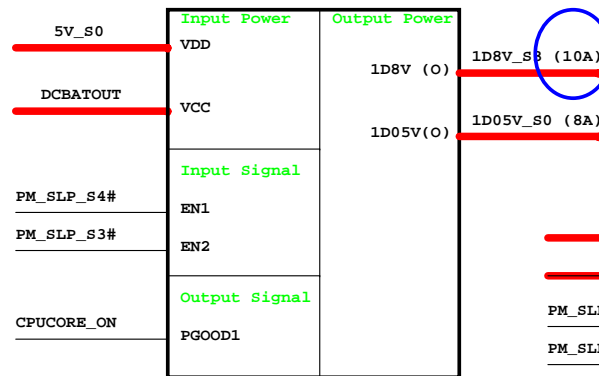
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
RUN POWER and 3D3V_AUX_S5			
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**CPU_CORE
MAX8770**

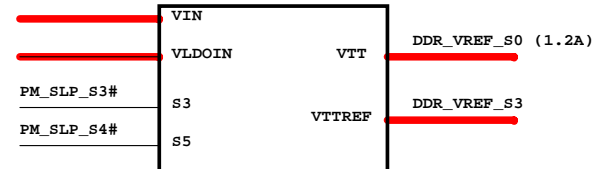


**MAX8717
1D8V_S3 / 1D05V_S0**

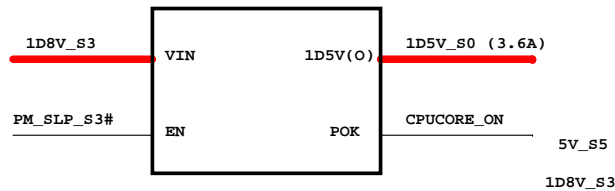
2007.1.19



**TPS51100
DDR_VREF_S0**



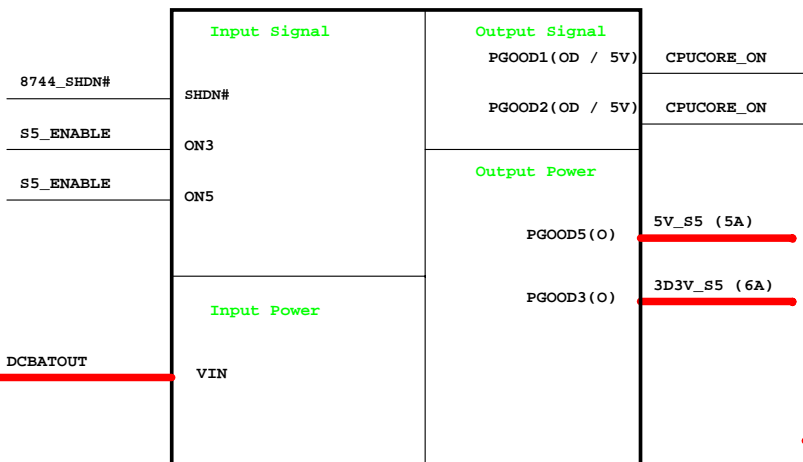
**APL5912
1D5V_S0**



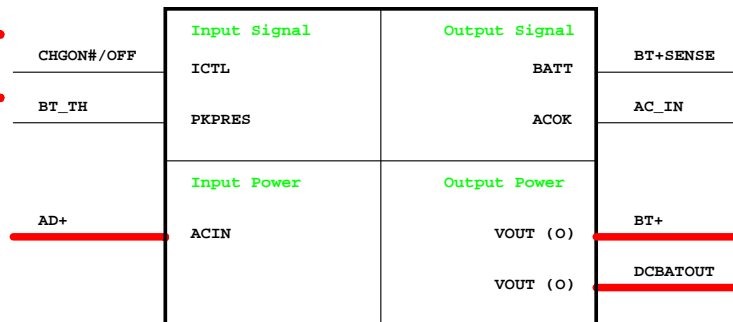
**APL5312
2D5V_S0**



**MAX8744
5V_S5 / 3D3V_S5**

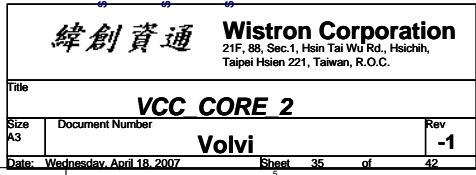


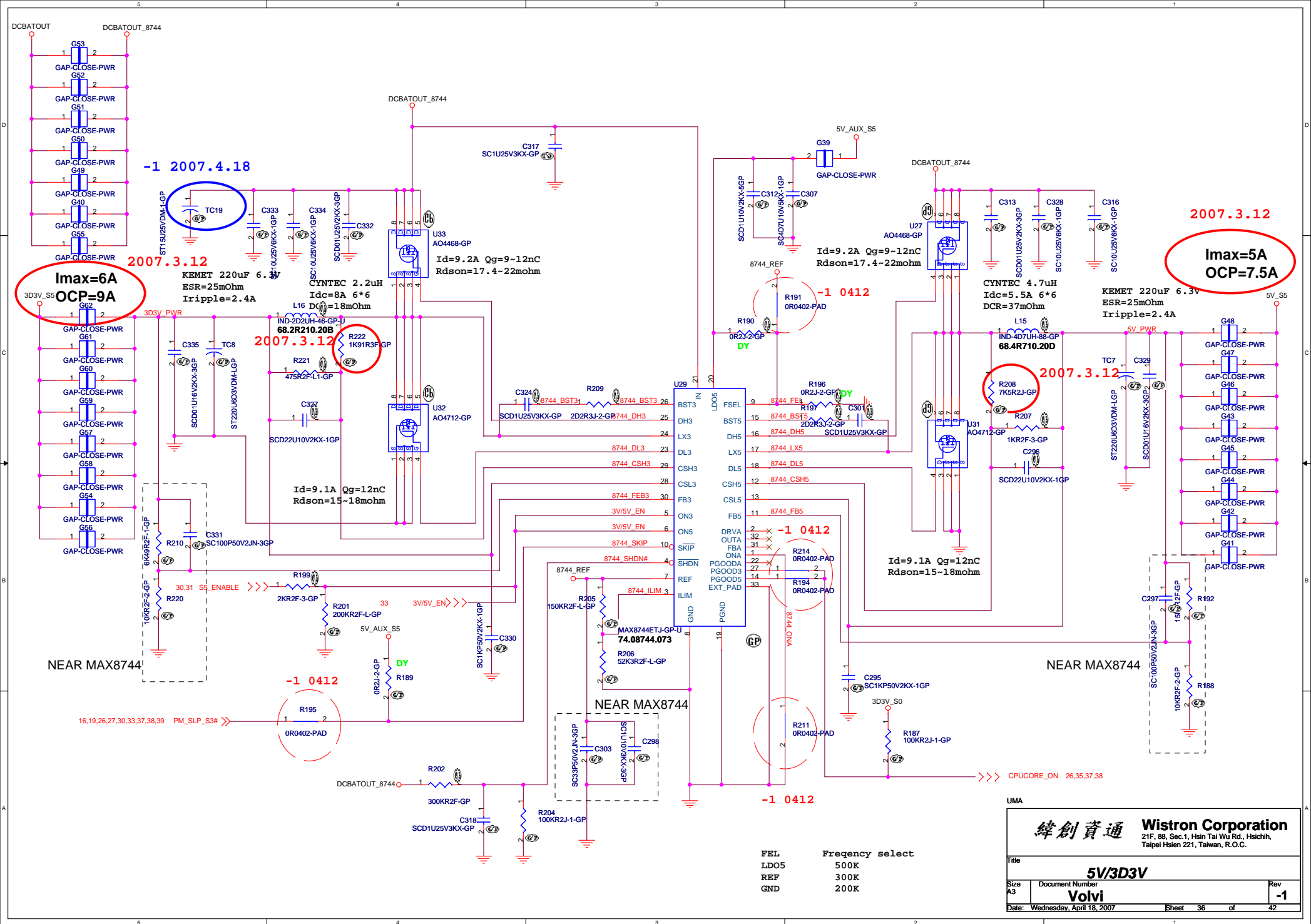
Charger MAX8731A



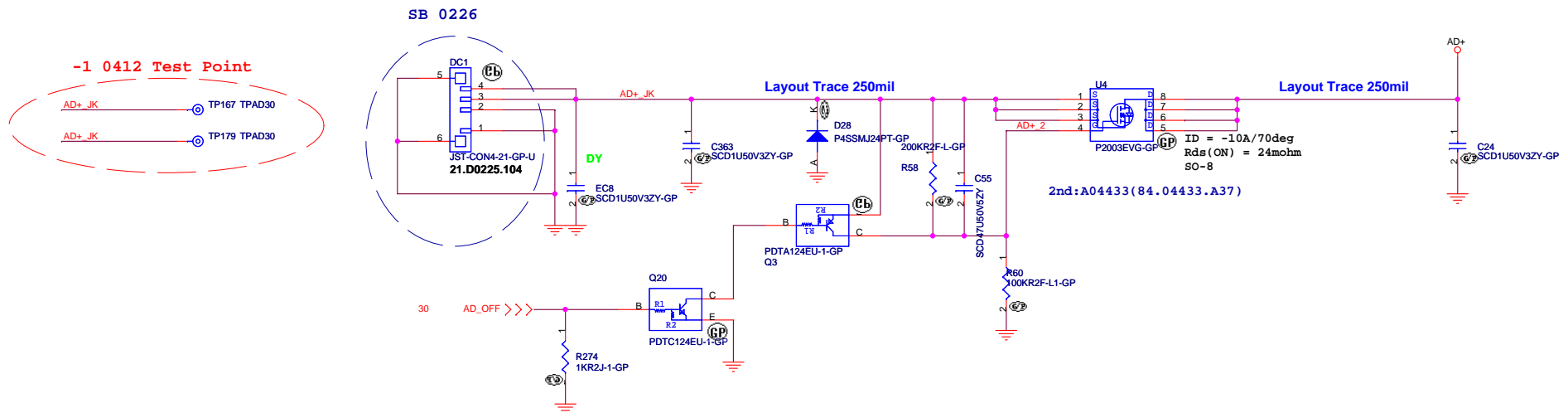
UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Power Block Diagram	
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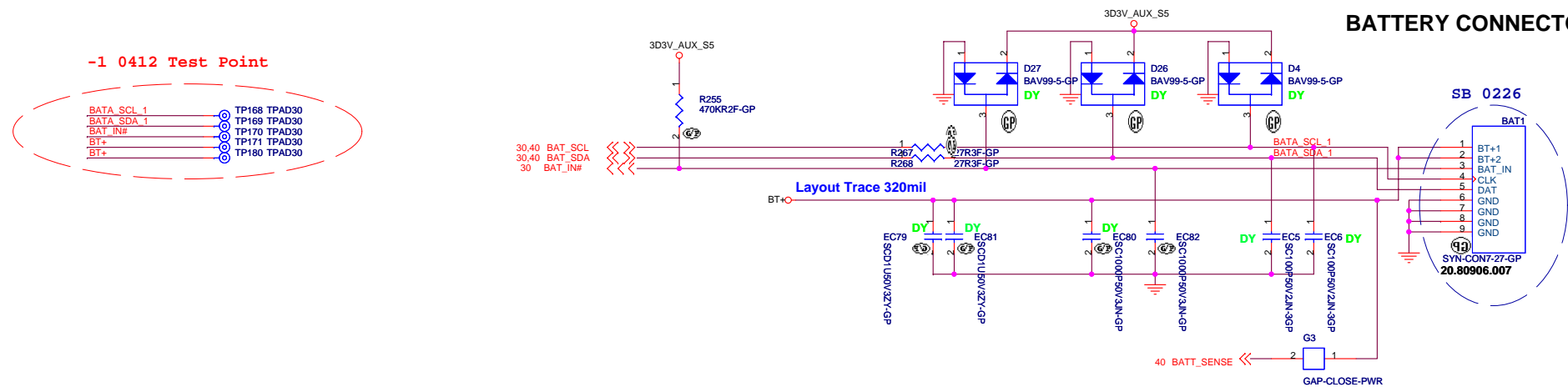




Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

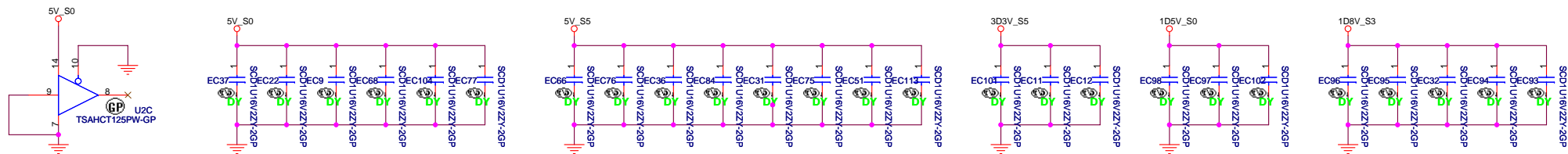


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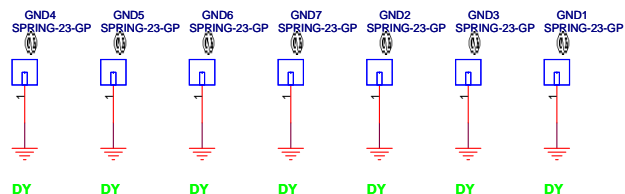
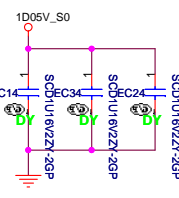
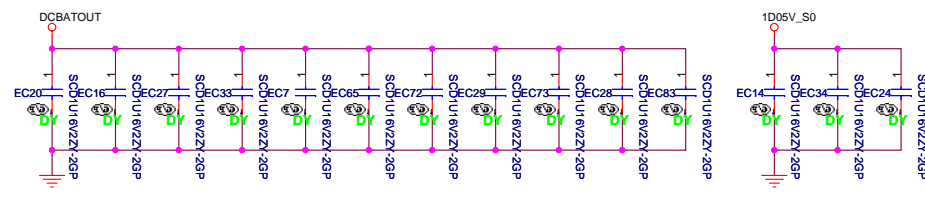
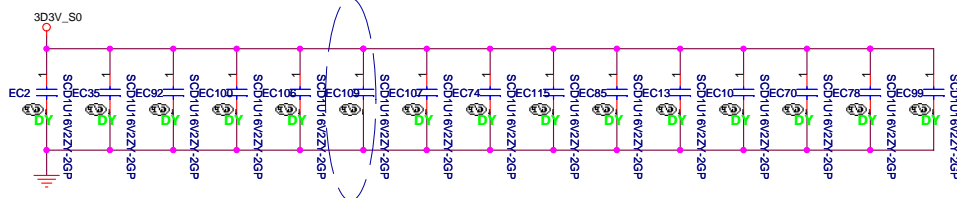
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Title		
AD/BATT CONN		
Size	Document Number	Rev
A3	Volvi	-1

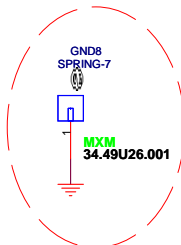
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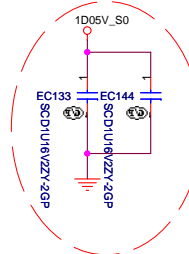
SB 0312 for EMI



-1 0413

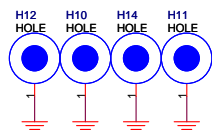


-1 0417 for EMI

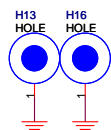


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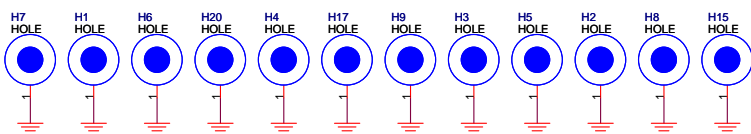
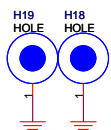
34.4T901.001



34.4T902.001



34.4T903.001



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Taipei Hsien 221, Taiwan, R.O.C.

Title		EMI/Spring/Boss	
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